MANGALORE UNIVERSITY

Department of Electronics

ELS 407 - VERILOG HDL

Course Outcome:-

1. Familiarize with the CAD tool to write HDL programs.
2. Design, simulate and synthesize digital logic circuits using Verilog HDL
3. Design sequential and combinational logic circuits for real-time applications.
4. Exposure to hardware-software co-design
5. Interface hardware to programmable logical devices like CPLDs/FPGAs/Microcontroller.

UNIT - I

Introduction: Overview of Digital Design with Verilog HDL Evolution of CAD, emergence of HDLs, typical HDL-flow, why Verilog HDL?, trends in HDLs.

Hierarchical Modeling Concepts: Top-down and bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block, stimulus block

Basic Concepts: Lexical conventions, data types, system tasks, compiler directives. Modules and Ports Module definition, port declaration, connecting ports, hierarchical name referencing.

12 Hours

UNIT - II

Gate Level Modeling: Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples, Tristate Gates, Array of Instances of Primitives, Design of Flip-Flops with Gate Primitives, Delay, Strengths and Construction Resolution, Net Types, Design of Basic Circuit.

Behavioral Modeling: Introduction, Operations and Assignments ,Functional Bifurcation, 'Initial' Construct, Assignments with Delays, 'Wait' Construct, Multiple Always Block, Designs at Behavioral Level, Blocking and Non-Blocking Assignments, The 'Case' Statement, Simulation Flow, 'If' an 'if-Else' Constructs, 'Assign- De-Assign' Constructs, 'Repeat' Construct, for loop, 'The Disable' Construct, 'While Loop', Forever Loop, Parallel Blocks, Force-Release, Construct, Event.

12 Hours

UNIT - III

Modeling at Dataflow Level: Introduction, Continuous Assignment Structure, Delays and Continuous Assignments, Assignment to Vector, Operators.

Sequential Circuit Description: Sequential Models - Feedback Model, Capacitive Model, Implicit Model, Basic Memory Components, Functional Register, Static Machine Coding, Sequential Synthesis.

Components Test and Verification: Test Bench - Combinational Circuits Testing, Sequential Circuit Testing, Test Bench Techniques, Design Verification, Assertion Verification.

12 Hours

Books:

1. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Pearson Education, Second Edition.
2. Digital Design (Verilog) An Embedded Systems Approach Using Verilog, Peter Ashenden, Elsevier Publications, 1st Edition 2008
3. Advanced Digital Design with Verilog HDL - Michel D. Ciletti, PHI,2009.
4. T.R. Padmanabhan, B Bala Tripura Sundari, Design Through Verilog HDL, Wiley 2009.